PATENT E1821-00001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Chung Zen Chen** Examiner: **Huan Hoang**

Serial No.: **10/792,120** Group Art Unit: **2827**

Filed: **March 3, 2004** Confirmation No.: **3928**

For: **BIT SWITCH VOLTAGE DROP COMPENSATION DURING PROGRAMMING NONVOLATILE MEMORY**

CERTIFICATION UNDER 37 C.F.R. §1.10

I hereby certify that this document (and the documents referred to as attached therein) is being deposited with the United States Postal Service on the date shown below with sufficient postage as "Express Mail Post Office to Addressee" Mailing Label Number EV690215644US to the following:

Dated: 9/13/05

Joseph A. Powers, Esq.
(Reg. No. 47,006)

INVENTOR DECLARATION UNDER RULE 1.132 OF CHUNG ZEN CHEN

I, Chung Zen Chen, declare the following:

1. I am the sole inventor of the subject matter described and claimed in U.S. patent Application No. 10/792,120 filed March 3, 2004, entitled "Bit Switch Voltage Drop Compensation During Programming in Nonvolatile Memory."

2. It has come to my attention that, through error and without any deceptive intent, a few factual errors were made in describing the simulation results in the "Detailed Description" section of the application as filed. I seek to correct these factual points by this declaration.

3. Paragraph [0032] of the application as filed should state that the tables illustrate that the bit line voltage VBL drops between about 0.4 to 0.6 volts compared with the regulated, fixed VDQ2 when between about "0.3-0.4 mA flows through a bit line" rather than when "2.5-3.3 mA current flows through the bit line or bit lines."

4. Also, Paragraph [0032] of the application as filed should state that the notation "0 mA" represents that "the selected cell to be programmed is in a programmed state and the other cells sharing the bit line have no leakage current during programming, or all of the cells in the selected bit line have no leakage current during overerase correction."

5. Further, Tables 1-1 and 1-2 should provide voltage VBL rather than voltage VDP, as described in preceding Paragraph 32. Tables 1-1 and 1-2 are provided in Appendix A to this Declaration with the simulation results showing voltage VBL referenced in Paragraph 32 of the application as filed.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further state that these statements were made with my knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this patent.

Dated: 9/13, 2005

Respectfully Submitted,

Chung Zen Chen

Chung Zen Chen

Appendix A

Table 1-1. VCC/Temp=3.6V/0°C; VR=1.2V.

VDQ1	VDQ2	No. of I/O to be programmed	total bit line current	G	VBL
6V	4.67V	1	0mA	5.2V	4.67V
	4.66V		0.315mA	5.07V	4.26V
	4.67V	8	0mA	5.2V	4.67V
	4.66V		2.53mA	4.81V	4.25V
8V	4.69V	1	0mA	7.24V	4.69V
	4.67V		0.317mA	7.10V	4.27V
	4.69V	8	0mA	7.24V	4.69V
	4.65V		2.52mA	6.86V	4.26V

Table 1-2. VCC/Temp=2.5V/90°C; VR=1.2V.

VDQ1	VDQ2	No. of I/O to be programmed	Total cell current	G	VBL
6V	4.68V	1	0mA	5.4V	4.68V
	4.66V		0.344mA	5.22V	4.11V
	4.68V	8	0mA	5.4V	4.68V
	4.65V		2.74mA	4.89V	4.11V
8V	4.70V	1	0mA	7.44V	4.70V
	4.67V		0.344mA	7.25V	4.12V
	4.70V	8	0mA	7.44V	4.70V
	4.65V		2.74mA	6.94V	4.10V